IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Karen L. NOEL et al.	Confirmation No.:	7142
Serial No.:	10/619,697	Group Art Unit:	2188
Filed:	07/15/2003	Examiner:	K. M. Patel
For:	Method and System of Writing Data In A Multiple Processor Computer System	Docket No.:	200312434-1

REPLY BRIEF

Mail Stop Appeal Brief – Patents   Date: March 7, 2007
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Examiner's Answer dated February 9, 2007, Appellants submit this Reply Brief.

I.   RESPONSE TO ARGUMENTS OF THE ANSWER

As stated throughout the Appeal Brief, Harvey teaches only replicating operating system code and read-only data as between processor memories. The "Response to Argument" section of the Examiner's Answer fully supports Appellants' position.

> Harvey further teaches that, "Still significant benefits can result if a replication policy is implemented selectively" by replicating operating system's code and read only data.

(Examiner's Answer, Paragraph (10), Page 6).

However, the Examiner's Answer makes what is effectively a obviousness argument under 35 USC § 103, stating:

> [A]ccordingly one having ordinary skill in the art at the time of the invention would be motivated to replicate any data (including writable data as claimed by applicant) that do no require any synchronization/coherency overhead to improve system performance by reducing non-uniform memory access times.

(*Id.* at Page 7).

With respect to claims 1 and 2, the rejections on appeal are anticipation rejections under 35 USC § 102. Thus, the question is not whether one of ordinary skill in the art would think to **modify** Harvey to replicate writeable data, as the Response to Arguments would suggest; rather, the question is whether Harvey expressly or inherently teaches the claimed limitations. The Response to Argument section admits as a matter of law that Harvey does expressly or inherently teach the claim limitations, but that some modification (based on ordinary skill) is needed. A clearly improper argument given the rejection currently being appealed.

Moreover, even if it is hypothetically assumed that such a modification is proper for the anticipation rejections (which Appellants do not admit) and generally with respect to the obviousness rejections, the modification itself is improper. The justification for modification is based on the teachings of the Appellants' Detailed Description. In particular, the Answer states:

> It is clear from the forgoing [sic] statements that read/write data (writable data of the applicant) carries significant overhead of maintaining synchronization/coherency, which can offset the advantage of reducing memory access costs, and as per applicant's specification, the writable data do not require such synchronization/coherency [citing Appellants' Detailed Description, Paragraph '0015].
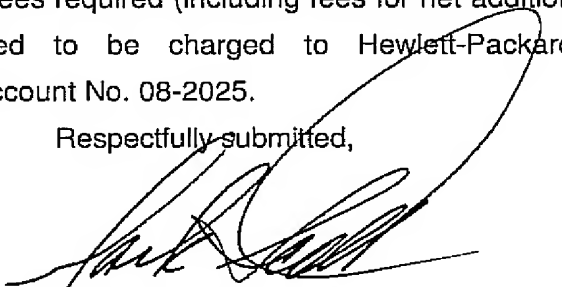
(Examiner's Answer, Paragraph (10), Page 7). The teachings of the Appellants' specification are not prior art, thus it is wholly improper to combine the Appellants' Detailed Description with other references to arrive at obviousness. Striking the portions of the Response to Argument that are clearly improper (obviousness arguments for anticipation rejections, and using Appellants' Detailed Description as prior art against them), the Response to Argument section merely buttresses Appellants' position that Harvey does not expressly or inherently teach the limitations of claims 1 and 2, and does not render obvious the remaining claims.

II. CONCLUSION

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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